## ***Amendments to the claims:***

1(Presently amended) An apparatus for the downloading of a code image to a wireless receiver, said apparatus having:

a Sequence Controller generating a ROM controller enable output and a CPU enable output;

a ROM ~~for the storage of~~ having a SRC value, a DST value, a LENGTH value, and a boot image;

a DMA controller ~~responsive to~~ having a SRC register specifying a source location, a DST register specifying a destination location, and a LENGTH register, said DMA controller ~~copying~~ moving an amount of data specified by said LENGTH register from ~~a~~ said source location ~~specified by SRC~~ to ~~a~~ said destination location ~~specified by DST for a duration specified by LENGTH~~;

a ROM controller coupled to said ROM, said ROM controller initializing said DMA controller upon assertion of said ROM controller enable output by copying said SRC value from said ROM to said DMA controller SRC register, said DST value from said ROM to said DMA controller DST register, and said LENGTH value from ~~the contents of~~ said ROM to said DMA controller LENGTH register;

a memory coupled to said DMA controller, said DMA controller copying at least part of said boot image from said ROM into said memory prior to the assertion of said CPU enable output; ~~responsive to said DST;~~

a CPU coupled to and executing instructions from said memory, said CPU enabled upon the assertion of said CPU enable output;

~~said CPU enable output asserted after said DMA controller has copied said ROM data to said memory;~~

a wireless front end coupled to said CPU, said CPU ~~downloading~~ executing instructions from said boot image causing said cpu to download and execute an operating system image from a source coupled to a wireless link accessed through said wireless front end. ~~for use by said CPU.~~

2(Original) The apparatus of claim 1 where said memory is a static random access memory.

3(Original) The apparatus of claim 1 where said memory is a dynamic random access memory.

4(Presently amended) The apparatus of claim 2 where said static random access memory is addressed by said SRC register.

5(Original) The apparatus of claim 3 where said CPU downloads said operating system image into said dynamic random access memory.

6(Original) The apparatus of claim 1 where said sequence controller uniquely asserts said ROM controller output and said CPU enable output.

7(Original) The apparatus of claim 1 where said sequence controller first asserts said ROM controller output, and asserts said CPU enable output after completion of copying of said LENGTH from said SRC to said DST.

8(Original) The apparatus of claim 1 where said boot image includes instructions for:

sending a download request;

receiving a packet accompanied by a sequence number;

discarding a packet with the same sequence number as an earlier-received packet;

accepting a packet with a unique sequence number;

sending a download request if a gap in sequence numbers is detected.

9(Original) The apparatus of claim 1 where a download server with a wireless interface receives a download request from a wireless client and responds to said download request by:

sending download data including a sequence number, each download data comprising an original packet and a duplicate packet each including said sequence number;

incrementing the sequence number for each subsequently sent download data;

upon sending all said download data, thereafter sending a "done" packet indicating completion of the download.

10(Presently amended) A process for the downloading of wireless code to a receiver, said process comprising:

a first step of copying a SRC value, a DST value, and a LENGTH value from a ROM to a DMA controller;

a second step of said DMA controller copying ~~additional data~~ instructions from said ROM ~~responsive to~~

referenced by said SRC ~~address~~ value to a memory ~~responsive~~ location referenced by ~~to~~ said DST value ~~address~~;

a third step of a CPU executing said instructions ~~located~~ placed into ~~in~~ said memory by said second step;

a fourth step of said CPU downloading an operating system program from a remote host using instructions placed in said memory by said third step, thereafter executing said operating system program.

11(Presently amended) The process of claim 10 where said SRC ~~address~~ value causes said DMA controller to read from ~~selects~~ a region in said ROM and said LENGTH defines a contiguous region of said ROM.

12(Presently amended) The process of claim 10 where said DST value causes said DMA controller to write to ~~corresponds to an address of~~ a region in said memory.

13(Original) The process of claim 10 where said third step said CPU instructions includes the instructions for:

transmitting a download request;

receiving a packet accompanied by a sequence number;

discarding a packet with the same sequence number as an earlier-received packet;

accepting a packet with a unique sequence number;

sending a download request if a gap in sequence numbers is detected.

14(Original) The process of claim 10 where said fourth step includes:

sending a download request;

receiving a packet accompanied by a sequence number;

discarding a packet with the same sequence number as an earlier-received packet;

accepting a packet with a unique sequence number;

sending a download request if a gap in sequence numbers is detected.

15(Original) The process of claim 10 where said remote host responds to said download request by:

sending download data including a sequence number, each download data comprising an original packet and a duplicate packet each including said sequence number;

incrementing the sequence number for each subsequently sent download data;

upon sending all said download data, thereafter sending a "done" packet indicating completion of the download.

16(Original) The process of claim 15 where said download data includes an operating system for use by said CPU.

17(Original) The process of claim 10 where said original and said duplicate packet are not interleaved.

18(Original) The process of claim 10 where said original and said duplicate packet are interleaved.

19(Original) The process of claim 10 where said duplicate packet includes a plurality of packets, each said packet having the same said Tx_Seq_Num as said original packet.

20-23 Cancelled.

24 (New claim) An apparatus for the downloading of a code image to a wireless receiver, said apparatus having:

a Sequence Controller generating a ROM controller enable output and a CPU enable output;

a ROM having a SRC value, a DST value, a LENGTH value, and a boot image;

a DMA controller having a SRC register specifying a source location, a DST register specifying a destination location, and a LENGTH register, said DMA controller moving an amount of data specified by said LENGTH register from ~~a~~ said source location to said destination location;

a ROM controller coupled to said ROM, said ROM controller initializing said DMA controller upon assertion of said ROM controller enable output by copying said SRC value from said ROM to said DMA controller SRC register, said DST value from said ROM to said DMA controller DST register, and said LENGTH value from said ROM to said DMA controller LENGTH register;

a memory coupled to said DMA controller, said DMA controller copying at least part of said boot image from said ROM into said memory;

a CPU coupled to said memory, said CPU enabled upon the assertion of said CPU enable output, said CPU enable output asserted after said DMA controller has moved said boot image from said ROM into said memory, said CPU thereafter executing said boot image from said memory.